

What is Claimed is:

1. An ATM slave interface unit providing an interface between an ATM master processing unit and an ATM slave processing unit, the interface unit comprising:

5 an input unit, the input unit receiving data cells and exchanging control signals with the ATM master processing unit;

an input buffer unit including:

a buffer storage unit; and

10 a calculation unit, wherein the input buffer unit receives data signals from and exchanges control signals with the input unit, the input buffer unit storing received data cells in the buffer storage unit, the buffer storage unit transferring data cells to the ATM slave processing unit; and

15 a register, each data cell including a cell location identifying a destination location, the calculation unit responsive to the contents of the register and to the data cell for generating a destination location control signal for the data cell.

2. The interface unit as recited in claim 1 wherein the buffer storage unit is a first-in/first-out memory unit.

20 3. The interface unit as recited in claim 1 wherein the first-in/first-out memory unit can store at least two data cells.

4. The interface unit as recited in claim 1 wherein the buffer storage unit transfers a data cell to the slave data processing unit every clock cycle.

25 5. The interface unit as recited in claim 1 wherein the destination locations can selected from the group consisting of a plurality of central processing unit, a plurality of memory locations, and at least one central processing unit and at least memory location.

30 6. The interface unit as recited in claim 1 further comprising:

an output buffer unit; the output buffer unit including a buffer storage unit, the buffer unit storing data cells, the output buffer unit receiving data cells from the slave processing unit, the data buffer unit exchanging control signals with the slave processing unit; and

an output unit; the output unit receiving data cells from the output buffer unit and applying data cells to the ATM master processing unit, the output unit exchanging control signals with the output buffer unit and with the ATM master processing unit.

7. The interface unit as recited in claim 1 wherein the ATM slave processing unit includes at least one digital signal central processing unit.

8. The interface unit as recited in claim 1 wherein the control signals and the data cells have the UTOPIA format.

9. The interface unit as recited in claim 1 wherein the ATM slave processing unit includes a direct memory access unit.

10. A method for exchanging data cells from an ATM master processing unit with a plurality of locations in an ATM slave processing unit, the method comprising:
storing data cells from the ATM master processing unit in a buffer storage unit;
comparing a field in the data cell with the contents of a register to determine the destination location of the data cell;
generating a signal identifying the destination location; and
when storage space is available, transferring a data cell from the buffer storage unit to the destination location.

11. The method as recited in claim 10 further comprising:
implementing the buffer storage to hold two data cells; and
transferring a data cell from the buffer storage unit to the ATM slave processing unit on consecutive clock cycles.

12. The method as recited in claim 11 further comprising implementing the control signals in a UTOPIA format.

13. The method as recited in claim 10 wherein the ATM slave processing unit includes a direct memory access unit, the method including applying the signal identifying the destination location to the direct memory access unit.

14. A data processing system comprising:

an ATM master processing unit;

an ATM slave processing unit; and

an ATM slave interface unit, the slave interface unit including:

an input unit, the input unit receiving data signals from the ATM master unit, the input unit exchanging control signals with the ATM master unit;

an input buffer storage unit, the input buffer unit including:

a memory unit; and

a calculation unit, wherein the input buffer unit exchanges control signals with the input unit, the input buffer unit storing data cells in the memory unit, the buffer storage unit transferring data cells to the ATM slave processing unit, the input buffer unit exchanging control signals with the ATM slave processing unit; and

a register, the contents of the register identifying the destination location field in a data cell, the contents of the register providing the translation of field in the data cell to a destination location, wherein the calculation unit generates a destination location signal and applies the destination location signal to the ATM slave processing unit.

15. The data processing system as recited in claim 14 wherein the ATM slave processing unit includes a direct memory access unit, the destination location signal being applied to the direct memory access unit.

16. The data processing system as recited in claim 14 wherein the memory unit is a first-in/first-out memory unit capable of storing at least two data cells.

17. The data processing system as recited in claim 16 wherein the input buffer unit transfers data cells to the ATM slave processing unit on consecutive lock cycles.

APPARATUS AND METHOD FOR AN INTERFACE UNIT FOR DATA TRANSFER BETWEEN A HOST PROCESSING UNIT AND A MULTI-CORE DIGITAL SIGNAL PROCESSING UNIT IN AN ASYNCHRONOUS TRANSFER MODE

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Abstract of the Disclosure

. A slave interface unit controls the exchange of data between a master processing
 unit and a plurality of slave processing units operating in the asynchronous transfer mode
 10 (ATM) of operation. The ATM slave interface unit has a receive unit and a transmit unit
 that exchange data cells and control signals with the ATM master processing unit. The
 receive unit and the transmit unit are coupled to a receive buffer storage unit and a
 transmit buffer storage unit, respectively. The receive buffer storage unit and the
 transmit buffer storage unit exchange data and control signals with the direct memory
 15 access unit. The ATM slave interface unit includes a configuration interface unit having
 a register that identifies the location in the data cell where the destination address is
 located and relates the destination address to the particular processing unit or memory
 location. The receive buffer unit uses the information in the register to determine the
 destination of the data cell.